Code No. 11249/O

FACULTY OF ENGINEERING

B.E. (I.T.) 4/4 I - Semester (Old) Examination, May / June 2019

Subject : VLSI Design

Time : 3 Hours Max. Marks: 75

Note: Answer all questions from Part-A & any five questions from Part-B.

PART – A (25 Marks)

1 Explain how a MOSFET works as a switch. (3)
2 Explain the operation of transmission gate logic. (3)
3 Draw the CMOS diagram of xor gate. (2)
4 Write about the layers used to create MOSFET. (2)
5 Write in brief about the stick diagrams? (3)
6 Explain Cell concepts briefly. (2)
7 Explain with a diagram Tri State circuit. (3)
8 What is propagation delay and write the expression for the same. (3)
9 Write the verilog code of half adder. (2)
10 Write in brief about testing. (2)

PART – B (50 Marks)

11 (a) Illustrate bubble pushing using De Morgan€s Law. (5)
(b) Draw the CMOS diagram of XOR and XNOR logic gate and explain with a truth table. (5)

12 (a) Draw the layout of three input NAND. (5)
(b) Write about photolithography. (5)

13 (a) Draw the DC characteristics of CMOS inverter and find the midpoint voltage. (4)
(b) With a neat diagram explain CMOS process flow for fabrication. (6)

14 (a) Explain read and write operation of DRAM cell. (5)
(b) Write about effect of charge storage on floating gate. (5)

15 (a) What is an interconnect? Derive the delay modeling of an interconnect. (5)
(b) Write the verilog code for full adder. (5)

16 (a) Design a 4 bit barrel shifter. (5)
(b) Write about multipliers. (5)

17 (a) Design an 8:1 MUX using 2:1MUX transmission gates. (5)
(b) Write about RTL and Behavioral modelling. (5)

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